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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/491,810 | 01/28/2000 | Thomas Justin Sullivan | 10981801-1 | 9074 |

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| EXAMINER | |
|---|---|
| MEONSKE, TONIA L | |
| ART UNIT | PAPER NUMBER |
| 2183 | 9 |

DATE MAILED: 06/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/491,810 | SULLIVAN, THOMAS JUSTIN | |
| | Examiner | Art Unit | |
| | Tonia L Meonske | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *05 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. Claims 1-3 are rejected under 35 U.S.C. 102(e) as being anticiapted by Roussel et al., US Patent 6,230,257 B1.

**3.** The rejections are respectfully maintained and incorporated by reference as set forth in the first office action, paper number 2, mailed on September 27, 2002.

### *Claim Rejections - 35 USC § 103*

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 4-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roussel et al., US Patent 6,230,257 B1, in view of Phillips et al, US Patent 6,038,652.

6. The rejections are respectfully maintained and incorporated by reference as set forth in the first office action, paper number 2, mailed on September 27, 2002.

### *Response to Arguments*

7. Applicant's arguments filed June 5, 2003 have been fully considered but they are not persuasive.

8. On pages 5-7, Applicant argues in essence :

*"The system apparenty disclosed in the '257 patent describes two single-precision ADD-execution units and two single-precision MUL-execution units. Two single-precision ADD-execution units and two single-precision MUL-execution units are not a single MAC unit as the office action suggests."*

However, in Figure 4A, the dashed box is the single MAC unit as claimed. The single dashed box performs multiplication and accumulation (Figure 4A, Column 4, See the add and multiply units.). Since the dashed box performs the breadth of the claim language of multiplication and accumulation, or addition, the dashed box is the claimed single MAC unit.

Furthermore, in an alternate embodiment, Roussel et al. have taught using a single MAC unit instead of separate add and multiply units to perform multiply-accumulate operations. (column 3, lines 39-41) In the alternate embodiment, the dashed box in Figure 4A is replaced by a single Multiply Accumulate Unit. (column 3, lines 39-41).

Therefore Roussel et al. have in fact taught a single MAC unit.

9. On pages 5-7, Applicant argues in essence :

*"The '257 patent fails to describe a single MAC unit configured in combination with the other recited elements as claimed. Consequently, for at least this reason, the '257 patent fails to disclose, teach, or suggest Applicant's claimed invention."*

However, in Figure 4A, the dashed box is the single MAC unit as claimed. The single dashed box performs multiplication and accumulation (Figure 4A, Column 4, See the add and multiply units.). Since the dashed box performs the breadth of the claim language of

multiplication and accumulation, or addition, the dashed box is the claimed single MAC unit.

Furthermore, in an alternate embodiment, Roussel et al. have taught using a single MAC unit instead of separate add and multiply units to perform multiply-accumulate operations. (column 3, lines 39-41) In the alternate embodiment, the dashed box in Figure 4A is replaced by a single Multiply Accumulate Unit. (column 3, lines 39-41). Therefore Roussel et al. have in fact taught a single MAC unit.

Furthermore Roussel et al. have taught this single MAC unit in combination with the other recited elements as claimed, such as:

(a) said single multiply accumulate (MAC) unit is configured to generate a data result responsive to a SIMD instruction (Abstract, Figure 3), the data result having a first half and a second half (Figure 3, column 3, lines 21-43, the first half, or low order, of the data result is (x1+y1)(x0+y0), the second half, or high order, of a data result is (x3+y3)( x2+y2), which are both generated from the single MAC unit.);

(b) a register communicatively coupled to the single MAC unit (Figure 4A, element M3), the register configured to store the first half of the data result. (column 4, lines 40-48, The low order results are held in delay element register M3.); and

(c) a miscellaneous (MISC) unit, said MISC unit determines when to release said first half of a data result stored in said defer

register to synchronize said first half of a data result with said second half of said data result. (column 4, lines 40-48,There is a MISC unit that determines when to write, or release, the results to the register file, depending upon when the high order results are ready. When the results of the first and second halves of the data result are written to the register file, the first half of the data result is "synchronized" with the second half of the data result.)

Therefore Roussel et al. have taught a single MAC unit configured in combination with the other recited elements as claimed.

10. On pages 9-10 Applicant argues in essence:

*"Passive delay units arranged to intercept data bytes on their way to an execution unit do not teach a register coupled to a MAC unit configured to store a data result. ... A register consists of a group of flip-flops and logic gates that effect their transition. The flip-flops hold binary information while the logic gates control when and how the binary information is transferred into the register."* (This argument is also repeated at pages 11 and 12.)

However, delay unit M3 is a register consisting of master slave flip flops (Column 7, lines 4-12, Column 8, lines 13-25, Element 400 in Figure 5 is the same as M3 in Figure 4A, as Figure 5 is the same as Figure 4a with additional bypassing functionality (Column 6, lines 37-54)). For further extrinsic evidence that a delay unit is a register, see Tomozawa, US Patent 3,979,701, with a publication date of September 7, 1976, and Evans, US Patent 3,761,922, with a publication date of September 25, 1973. This evidence supports the examiner's position that the prior art definition of a delay element in the context of this system is a register, and this definition has been known since at least 1973. Furthermore, the delay elements of Roussel et al. store a value which is read out

sometime later. (Column 4, lines 35-57, column 7, lines 11-14) Specifically, M3 stores a value and then the value is read once the high order results are ready. A register is something that merely holds or stores information for some period of time. Since the delay element, M3 of Roussel et al., holds the low order results with flip-flops, M3 is a register. Therefore Roussel et al. have in fact taught a register (Figure 4A, element M3, Figure 5, element 400) coupled to a MAC unit (Figure 4A, dashed box) configured to store a data result (column 4, lines 40-48, The low order results are held in delay element register M3.).

11. On pages 10-11, Applicant argues in essence:

*"...the '652 patent does not describe "applying an exception result as the input of the buffer when the miscellaneous-logic unit determines that the first half of the data result and the second half of the data result are invalid", as claimed in claim 6, and similarly claimed in claim 11."* (This argument is also repeated at pages 12 and 13.)

However, Phillips et al. was not solely cited as having taught "applying an exception result as the input of the buffer when the miscellaneous-logic unit determines that the first half of the data result and the second half of the data result are invalid." Roussel et al. in combination with Phillips et al., have taught "applying an exception result as the input of the buffer when the miscellaneous-logic unit determines that the first half of the data result and the second half of the data result are invalid."

Phillips et al. have taught that overflow or other exceptions may occur during multiply and accumulate functions and that it is necessary to report the exception in an efficient manner so that appropriate action can be taken (column 1, lines 20-46, column 4, lines 29-39). Generating an exception result and inputting, or forwarding, said exception result into a buffer if the operand data's are invalid is an efficient way to correct the exception

because the exception is immediately treated upon detection (Column 3, lines 44-62, Column 3, lines 44-62, Phillips et al. have taught reporting the exception in an exception flag/indicator bit in storage.). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the method for performing SIMD instructions, as taught by Roussel et al., include the concept of exception reporting to a buffer, as taught by Phillips et al., so that the invention of Roussel et al. includes: generating an exception result by said by a MISC unit; inputting said first operand data result and said second operand data result into a buffer if said MISC logic determines that said first operand data result and said second operand data result are valid; and inputting said exception result into said buffer if said MISC unit determines that said first operand data result and said second operand data result are invalid, so that when an exception occurs, the exception can be reported to the buffer, or an exception flag/indicator bit in a storage, and the exception can be corrected immediately in an efficient manner.

***Conclusion***

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L Meonske whose telephone number is (703) 305-3993. The examiner can normally be reached on Monday-Friday, 9-6:30, with every other Friday off.

13. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P Chan can be reached on (703) 305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

14. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

RICHARD L. ELLIS
PRIMARY EXAMINER

tlm
June 23, 2003